

FORM PTO-892 (REV. 3-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. <b>697830</b>	GROUP/UNIT <b>258</b>	ATTACHMENT TO PAPER NUMBER <b>2</b>
NOTICE OF REFERENCES CITED				APPLICANT(S) <b>Huang et al</b>		

  

U.S. PATENT DOCUMENTS							
*	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
A	4 916 498	4/10/80	Berenz	357	22A	Z	
B	4 821 093	4/11/89	Iafrate et al	357	22A		
C	4 600 932	7/15/86	Norris	357	22A		
D	4 652 896	3/24/87	Das et al	357	22A		
E	5 008 717	4/16/91	Bar-Joseph et al	357	22A		
F							
G							
H							
I							
J							
K							

  

FOREIGN PATENT DOCUMENTS							
*	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG. OR SPEC.
-L	1-19 9475	8/89	Japan	Matsumoto	357	22A	Z
-M	63-3 18165	12/88	Japan	Yamane	357	22A	
-N	59-1 19768	7/84	Japan	Ishikawa	357	22MD	
-O	59-4 085	1/84	Japan	Mutou	357	22MD	
-P	1-94 674	4/89	Japan	Nagami	357	22A	
-Q	1-128 473	5/89	Japan	Inoue	357	22A	

  

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)	
R	IEEE Electron Device Letters, Vol. 10, No. 10, October 1989, "A 0.25-um Gate- Length Pseudomorphic HFET with 32-mW Output Power at 94 GHz" by Smith et al, P. 437-P. 439.
T	IEEE Electron Device Letters, Vol. 11, No. 1, January 1990, "W-Band Low-Noise InAlAs/InGaAs Lattice-Matched HEMT's" by Chao et al, P. 59-P. 62.

  

EXAMINER <b>Loke</b>	DATE <b>10/16/91</b>
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\* A copy of this reference is not being furnished with this office action.  
(See Manual of Patent Examining Procedure, section 707.05 (a).)